WHAT IS CLAIMED IS:

1. A semiconductor device, comprising a thin film transistor including a semiconductor layer that includes a channel region, a source region and a drain region, a gate insulating film provided on the semiconductor layer, and a gate electrode for controlling a conductivity of the channel region, wherein a surface of the semiconductor layer includes a protruding portion, and a side surface inclination angle of the gate electrode is larger than an inclination angle of the protruding portion of the semiconductor layer.

2. A semiconductor device, comprising a thin film transistor including a semiconductor layer that includes a channel region, a source region and a drain region, a gate insulating film provided on the semiconductor layer, and a gate electrode for controlling a conductivity of the channel region, wherein the semiconductor layer includes a protruding portion, a cross-sectional shape of the gate electrode includes a first step portion and a second step portion provided on the first step portion, and a side surface inclination angle of each of the first and second step portions is larger than an inclination angle of the protruding portion of the semiconductor layer.

3. The semiconductor device according to claim 2,

wherein the gate electrode includes a first conductive film provided on the gate insulating film and a second conductive film provided on the first conductive film, a width of the first conductive film is larger than that of the second conductive film, and the first and second conductive films form the first and second step portions, respectively.

4. The semiconductor device according to claim 1, wherein a surface of the semiconductor layer includes a plurality of protruding portions, and a side surface inclination angle of the gate electrode is larger than an inclination angle of any of the plurality of protruding portions of the semiconductor layer.

5. The semiconductor device according to claim 2, wherein a surface of the semiconductor layer includes a plurality of protruding portions, a side surface inclination of each of the first and second step portions of the gate electrode is larger than an inclination angle of any of the plurality of protruding portions of the semiconductor layer.

6. The semiconductor device according to claim 1, wherein a side surface inclination angle of the gate electrode is about 75° to about 90°.

7. The semiconductor device according to claim 2, wherein a side surface inclination of each of the first and second step portions of the gate electrode is about 75° to about 90°.

8. The semiconductor device according to claim 1, wherein an inclination angle of the protruding portion of the semiconductor layer is about 30° to about 70°.

9. The semiconductor device according to claim 2, wherein an inclination angle of the protruding portion of the semiconductor layer is about 30° to about 70°.

10. The semiconductor device according to claim 1, wherein an average height of the protruding portion is about 8 nm to about 60 nm.

11. The semiconductor device according to claim 2, wherein an average height of the protruding portion is about 8 nm to about 60 nm.

12. The semiconductor device according to claim 1, wherein an average surface roughness of a surface of the semiconductor layer is about 4 nm to about 30 nm.

13. The semiconductor device according to claim 2, wherein an average surface roughness of a surface of the semiconductor layer is about 4 nm to about 30 nm.

14. The semiconductor device according to claim 1, wherein the semiconductor layer is formed from a crystalline semiconductor film, and the protruding portion is located over a boundary between crystal grains included in the semiconductor layer.

15. The semiconductor device according to claim 14, wherein the crystal grain boundary is a multipoint where three or more crystal grains meet.

16. The semiconductor device according to claim 14, wherein grain diameters of the crystal grains included in the semiconductor layer are about 100 nm to about 1000 nm.

17. The semiconductor device according to 14, wherein the crystal grain boundary is visualized through an etching process by a Secco etching method.

18. The semiconductor device according to claim 2, wherein the semiconductor layer is formed from a crystalline semiconductor film, and the protruding portion is located

over a boundary between crystal grains included in the semiconductor layer.

19. The semiconductor device according to claim 18, wherein the crystal grain boundary is a multipoint where three or more crystal grains meet.

20. The semiconductor device according to claim 18, wherein grain diameters of the crystal grains included in the semiconductor layer are about 100 nm to about 1000 nm.

21. The semiconductor device according to 18, wherein the crystal grain boundary is visualized through an etching process by a Secco etching method.

22. The semiconductor device according to claim 1, wherein the semiconductor layer is a crystalline semiconductor layer formed through a melting/solidification process, and the protruding portion is formed through the melting/solidification process.

23. The semiconductor device according to claim 2, wherein the semiconductor layer is a crystalline semiconductor layer formed through a melting/solidification process, and the protruding portion is formed through the

melting/solidification process.

24. The semiconductor device according to claim 1, wherein at least a portion of the semiconductor layer includes a catalyst element capable of promoting crystallization of an amorphous semiconductor film.

25. The semiconductor device according to claim 24, wherein the catalyst element is one or more element selected from the group consisting of nickel (Ni), iron (Fe), cobalt (Co), tin (Sn), lead (Pb), ruthenium (Ru), rhodium (Rh), palladium (Pd), osmium (Os), iridium (Ir), platinum (Pt), copper (Cu) and gold (Au).

26. The semiconductor device according to claim 2, wherein at least a portion of the semiconductor layer includes a catalyst element capable of promoting crystallization of an amorphous semiconductor film.

27. The semiconductor device according to claim 26, wherein the catalyst element is one or more element selected from the group consisting of nickel (Ni), iron (Fe), cobalt (Co), tin (Sn), lead (Pb), ruthenium (Ru), rhodium (Rh), palladium (Pd), osmium (Os), iridium (Ir), platinum (Pt), copper (Cu) and gold (Au).

28. The semiconductor device according to claim 1, wherein the semiconductor layer is a crystalline semiconductor film made up primarily of regions that are oriented along <111> crystal zone planes.

29. The semiconductor device according to claim 28, wherein about 50% or more of the regions that are oriented along the <111> crystal zone planes are regions that are oriented along a (110) plane or a (211) plane.

30. The semiconductor device according to claim 2, wherein the semiconductor layer is a crystalline semiconductor film made up primarily of regions that are oriented along <111> crystal zone planes.

31. The semiconductor device according to claim 30, wherein about 50% or more of the regions that are oriented along the <111> crystal zone planes are regions that are oriented along a (110) plane or a (211) plane.

32. The semiconductor device according to claim 1, wherein domain diameters of crystal domains of the semiconductor layer are about 2 μm to about 10 μm.

33. The semiconductor device according to claim 2, wherein domain diameters of crystal domains of the semiconductor layer are about 2 μm to about 10 μm.

34. The semiconductor device according to claim 1, wherein a lightly-doped impurity region is provided at a junction between the channel region and the source or drain region of the semiconductor layer.

35. The semiconductor device according to claim 2, wherein a lightly-doped impurity region is provided at a junction between the channel region and the source or drain region of the semiconductor layer.

36. The semiconductor device according to claim 2, wherein the first step portion of the gate electrode is present in a lightly-doped impurity region.

37. The semiconductor device according to claim 3, wherein the gate electrode is located above the channel region, and only the first conductive film of the gate electrode is present in a lightly-doped impurity region.

38. A method for manufacturing a semiconductor device, comprising the steps of:

(a) providing a semiconductor film;

(b) melting and solidifying the semiconductor film so as to obtain a crystalline semiconductor layer including a protruding portion on a surface thereof;

(c) forming a gate insulating film on the crystalline semiconductor layer;

(d) depositing a conductive film on the gate insulating film; and

(e) patterning the conductive film to form a gate electrode for controlling a conductivity of the channel region, wherein a side surface inclination angle of the gate electrode is larger than an inclination angle of the protruding portion on the surface of the crystalline semiconductor layer.

39. The method for manufacturing a semiconductor device according to claim 38, wherein the semiconductor film is an amorphous semiconductor film.

40. The method for manufacturing a semiconductor device according to claim 38, wherein the step (a) includes a step of performing a first heat treatment on an amorphous semiconductor film with a catalyst element capable of promoting crystallization thereof being added to at least a portion thereof so as to crystallize at least a portion of

the amorphous semiconductor film, thereby providing a semiconductor film including a crystalline region, and the step (b) includes a step of melting and solidifying a semiconductor film including the crystalline region so as to obtain a semiconductor film that includes a crystalline region including a protruding portion on a surface thereof.

41. The method for manufacturing a semiconductor device according to claim 38, wherein the step (d) includes the steps of:

(d-1) depositing a first conductive film on the gate insulating film; and

(d-2) depositing a second conductive film on the first conductive film.

42. The method for manufacturing a semiconductor device according to claim 38, wherein the step (e) includes:

a first step (e-1) of etching the second conductive film so that the second conductive film has a first side surface inclination angle;

a second step (e-2) of etching the first conductive film so that the first conductive film has a second side surface inclination angle; and

a third step (e-3) of further selectively etching the second conductive film, which has been etched so

that the second conductive film has the first side surface inclination angle, so that the second conductive film has a third side surface inclination angle that is larger than the first side surface inclination angle,

wherein the second side surface inclination angle and the third side surface inclination angle are each larger than the inclination angle of the protruding portion on the surface of the crystalline semiconductor layer.

43. The method for manufacturing a semiconductor device according to claim 42, wherein the step (e-1), the step (e-2) and the step (e-3) of the step (e) are performed continuously in an etching apparatus.

44. The method for manufacturing a semiconductor device according to claim 42, wherein the step (e) includes, performing between the step (e-2) and the step (e-3), a step of doping a portion of the crystalline semiconductor layer with an impurity element giving n-type or p-type conductivity using the etched second conductive film and the etched first conductive film as a mask.

45. The method for manufacturing a semiconductor device according to claim 42, further comprising, after the step

(e), a step (f) of doping a portion of the island-shaped semiconductor layer with an impurity element giving n-type or p-type conductivity using the gate electrode as a mask.

46. The method for manufacturing a semiconductor device according to claim 45, wherein the step (f) includes a step (f-1) of performing the doping step through the first conductive film using the second conductive film of the gate electrode as a mask.

47. The method for manufacturing a semiconductor device according to claim 46, wherein the step (f) includes the steps of:

(f-1a) doping a low concentration of the impurity element giving n-type or p-type conductivity through the first conductive film using the second conductive film of the gate electrode as a mask; and

(f-2) doping a high concentration of the impurity element giving n-type or p-type conductivity using the first conductive film of the gate electrode as a mask.

48. The method for manufacturing a semiconductor device according to claim 47, wherein the step (f-1a) and the step (f-2) are performed simultaneously, and the low concentration in the step (f-1a) and the high concentration in the step (f-

2) are controlled by a total thickness of the first conductive film and the second conductive film and a thickness of the first conductive film, respectively.

49. The method for manufacturing a semiconductor device according to claim 42, further comprising, after the step (f), a step of etching away exposed regions of the first conductive film using the second conductive film of the gate electrode as a mask.

50. The method for manufacturing a semiconductor device according to claim 38, wherein the step (e) is performed by an ICP etching method.

51. The method for manufacturing a semiconductor device according to claim 38, wherein the step (e) is performed by an RIE method.

52. The method for manufacturing a semiconductor device according to claim 42, wherein the step (b) includes a step of irradiating the semiconductor film with laser light.

53. The method for manufacturing a semiconductor device according to claim 52, wherein the laser light irradiation step is performed so that any point on the semiconductor film

is irradiated with pulsed laser light a plurality of times continuously.

54. The method for manufacturing a semiconductor device according to claim 40, wherein the catalyst element is one or more element selected from the group consisting of nickel (Ni), iron (Fe), cobalt (Co), tin (Sn), lead (Pb), ruthenium (Ru), rhodium (Rh), palladium (Pd), osmium (Os), iridium (Ir), platinum (Pt), copper (Cu) and gold (Au).

55. An electronic device, comprising the semiconductor device according to claim 1.

56. The electronic device according to claim 55, further comprising a display section where an image is displayed by using the semiconductor device.

57. An electronic device, comprising the semiconductor device according to claim 2.

58. The electronic device according to claim 57, further comprising a display section where an image is displayed by using the semiconductor device.